

FIG. 1

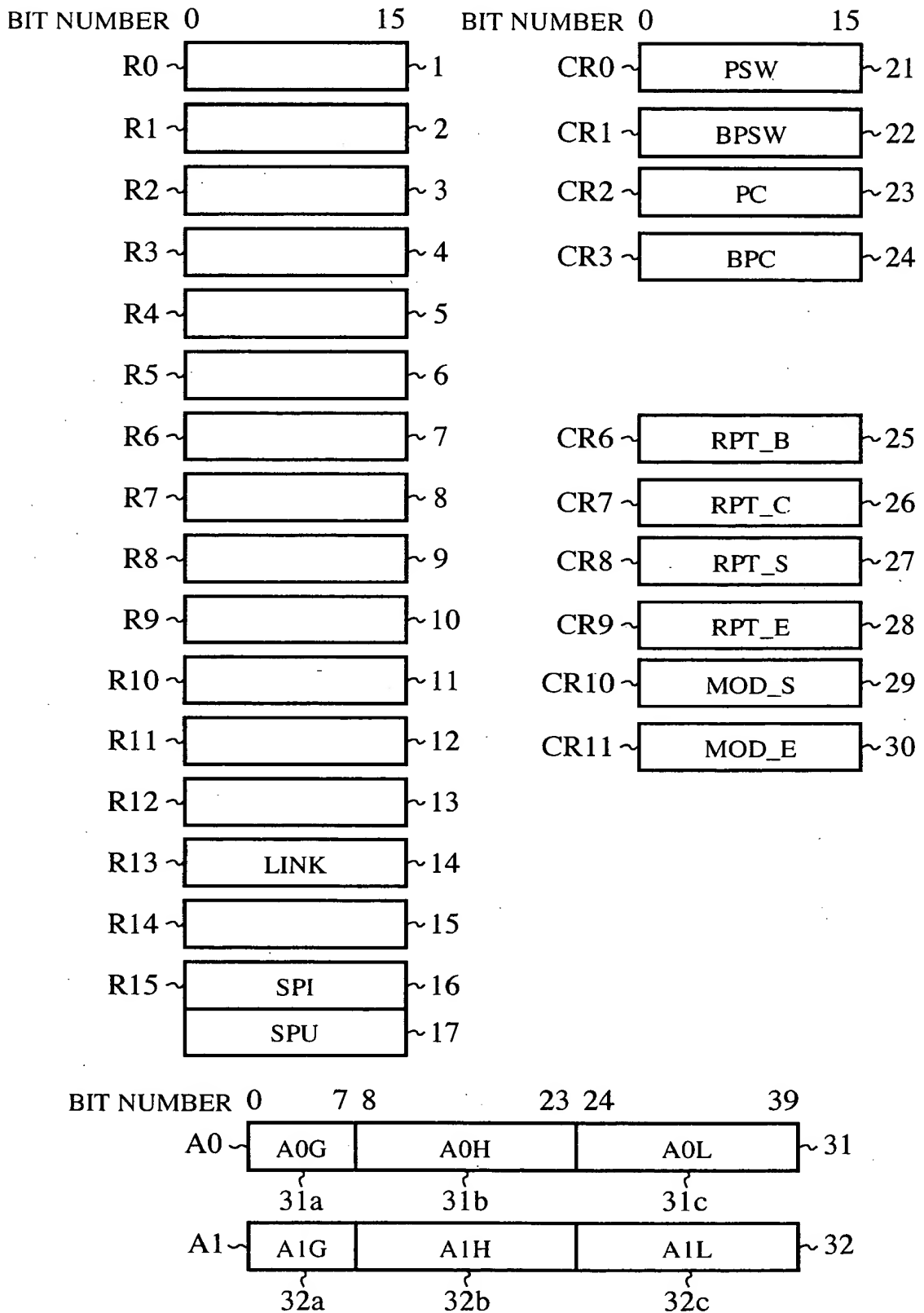


FIG.2

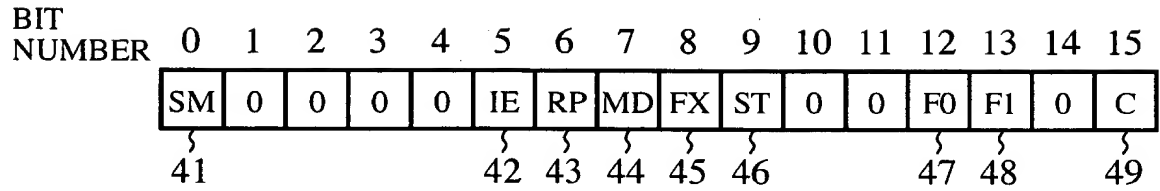


FIG.3

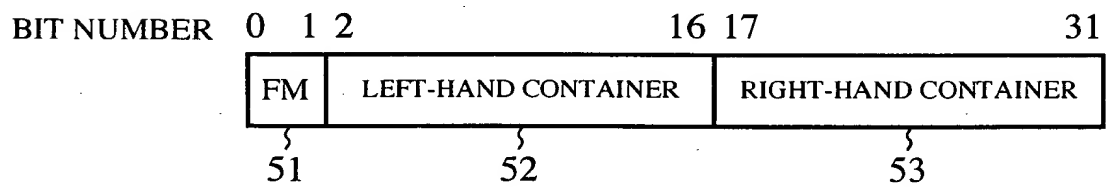


FIG.4

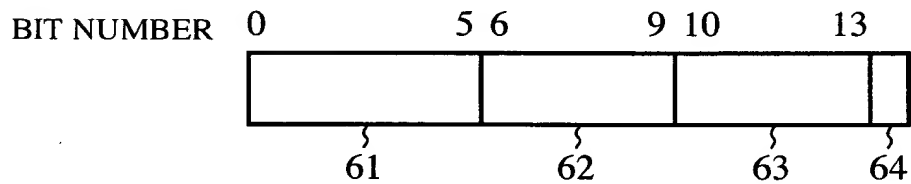


FIG.5

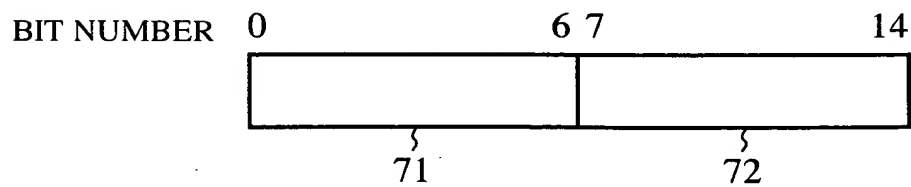


FIG. 2

FIG.6

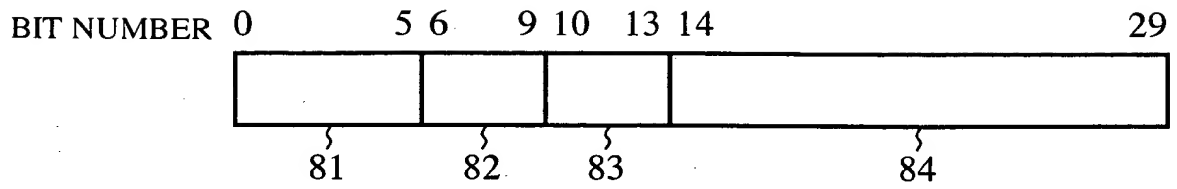


FIG.7

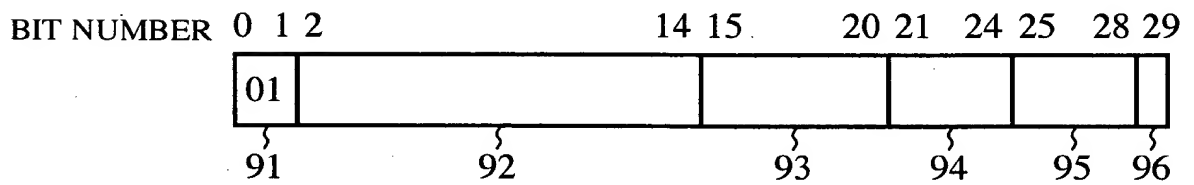


FIG.8

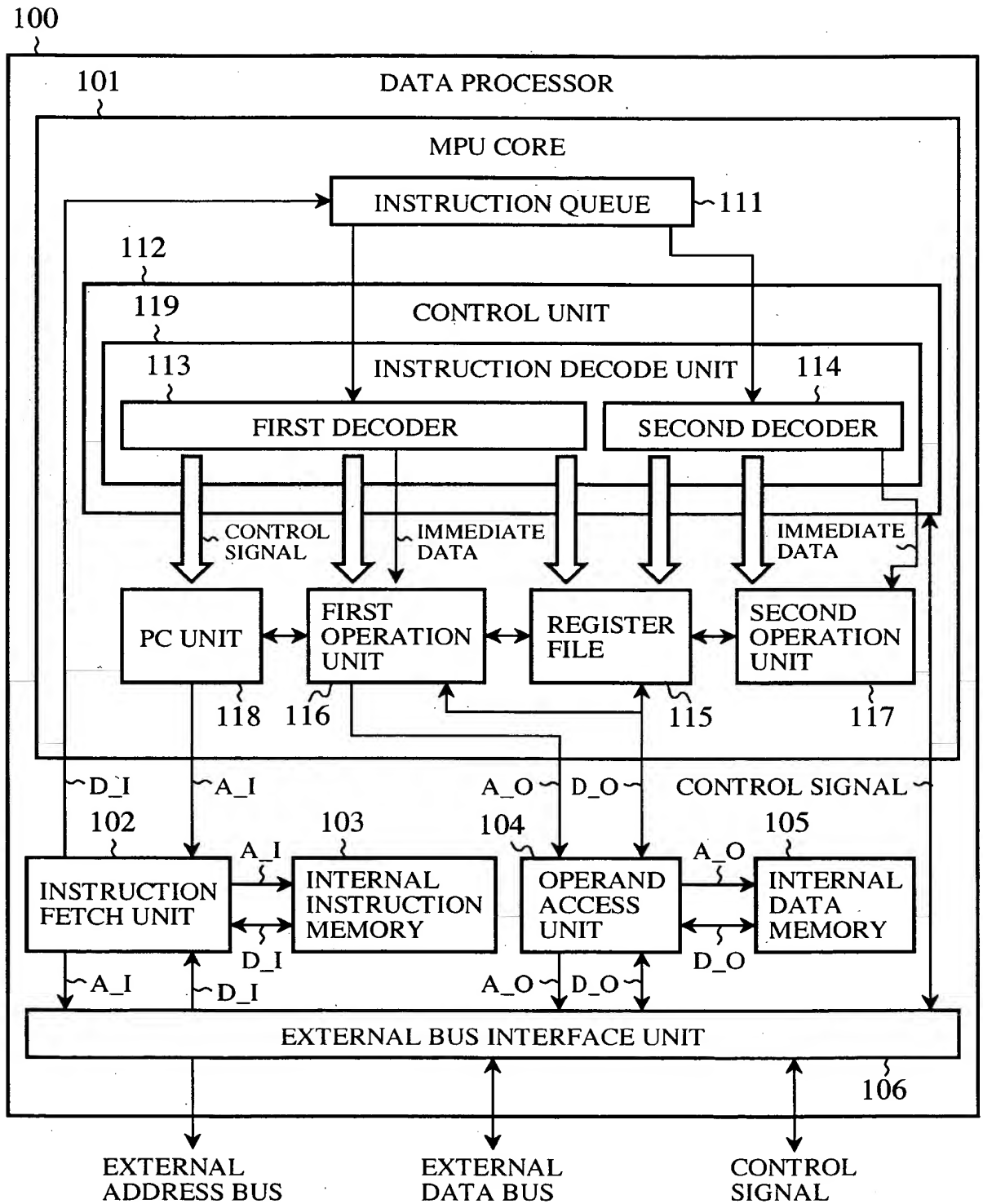


FIG.9

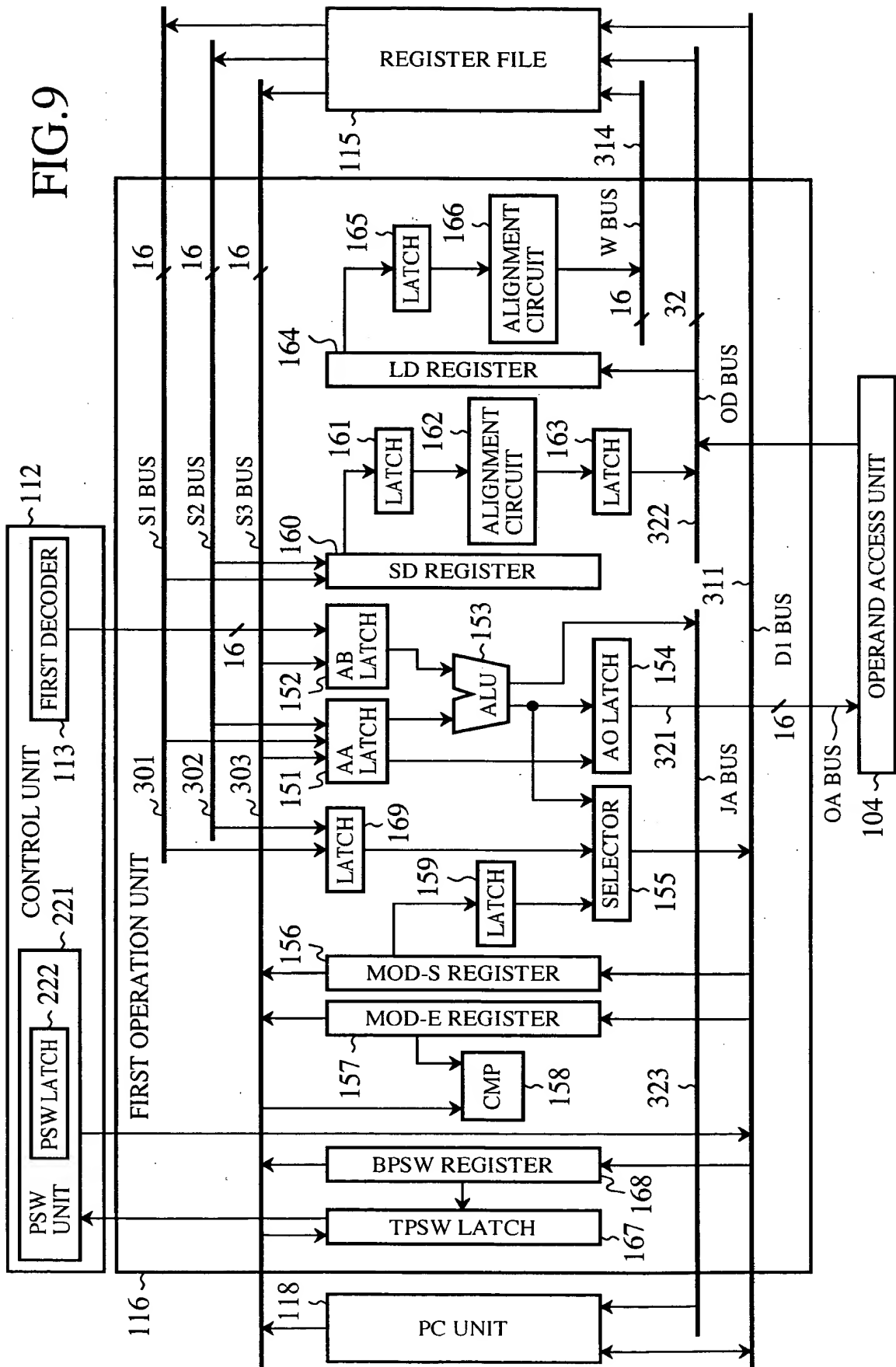


FIG. 10

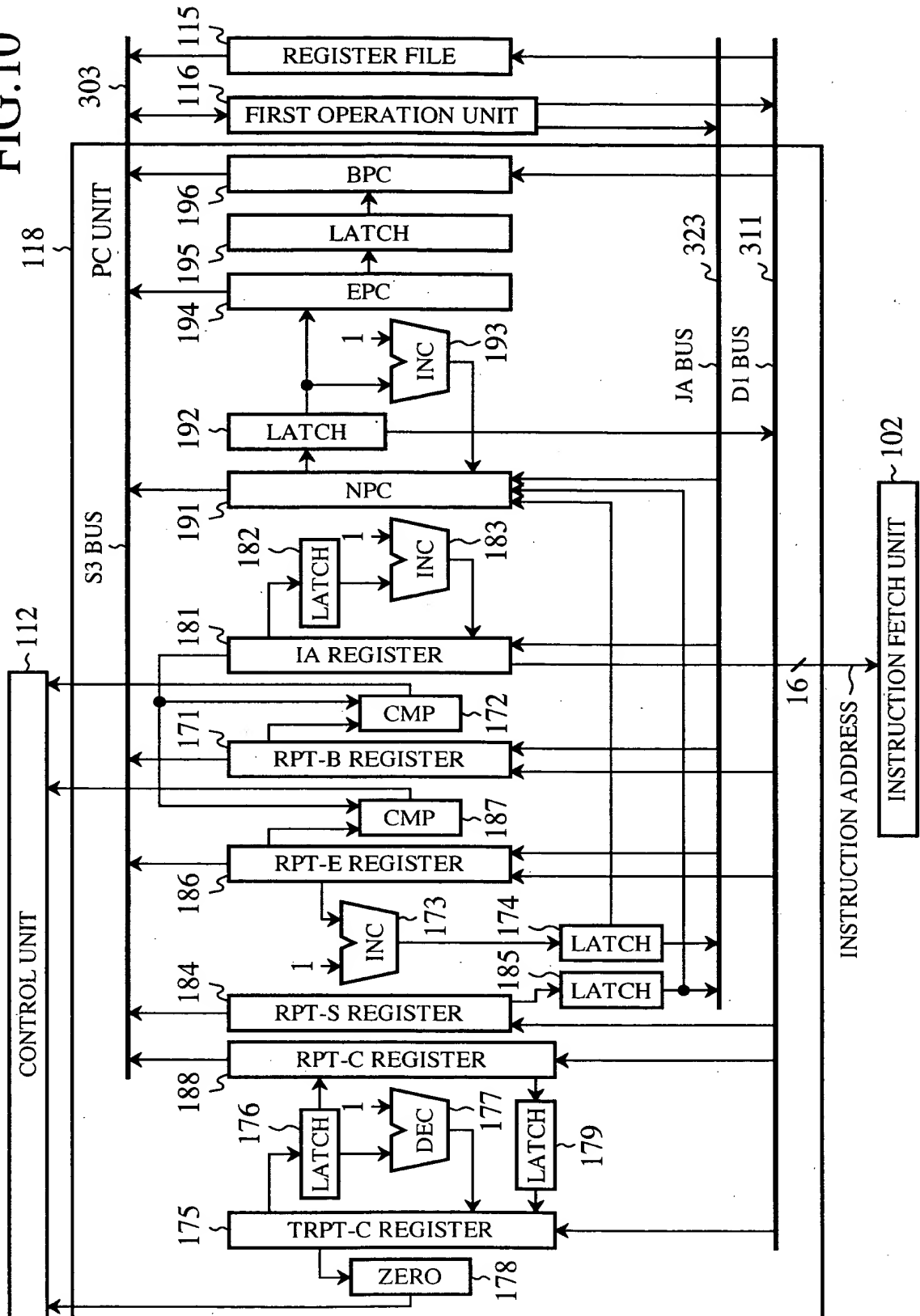


FIG. 11

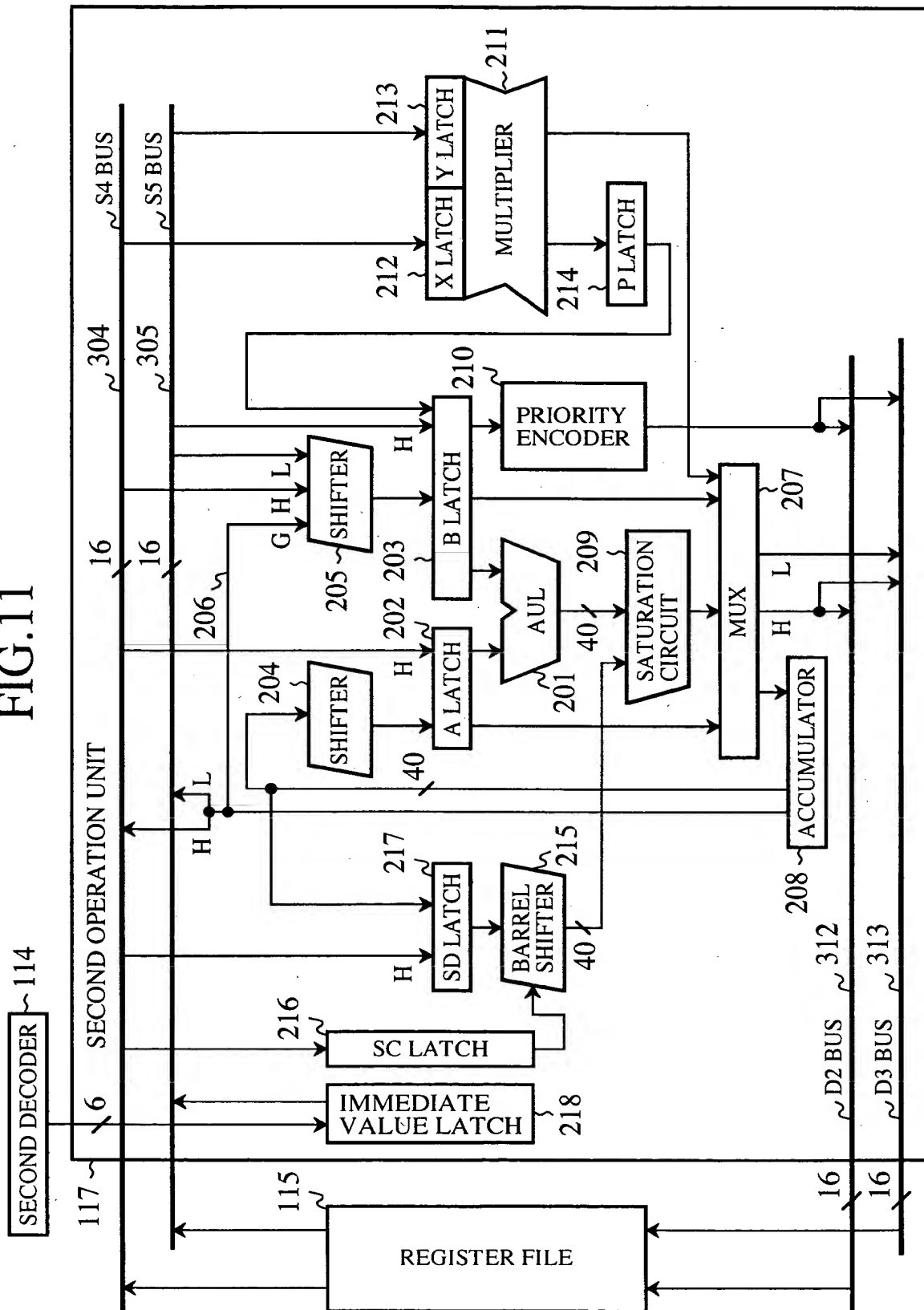


FIG. 12

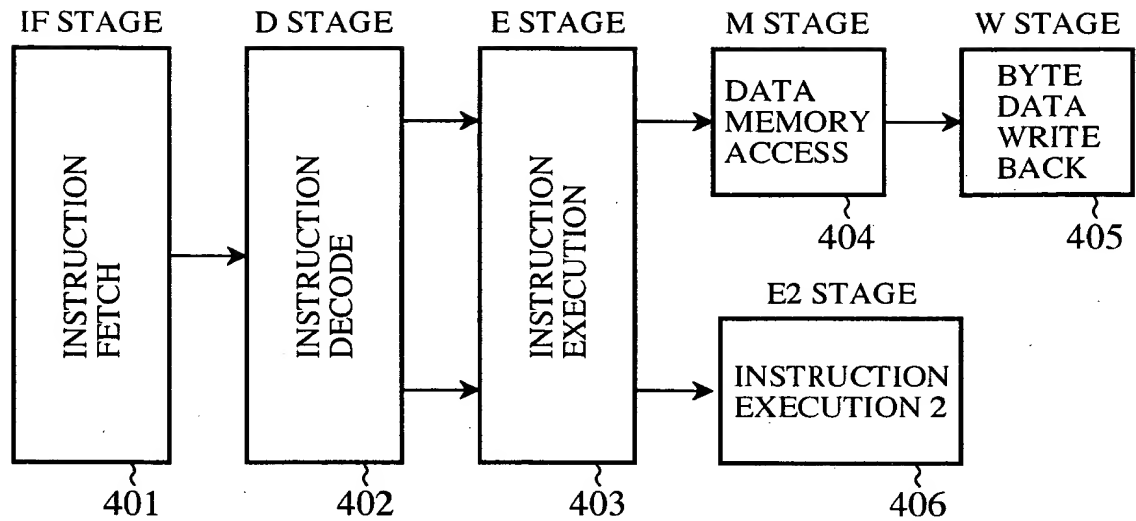


FIG. 13

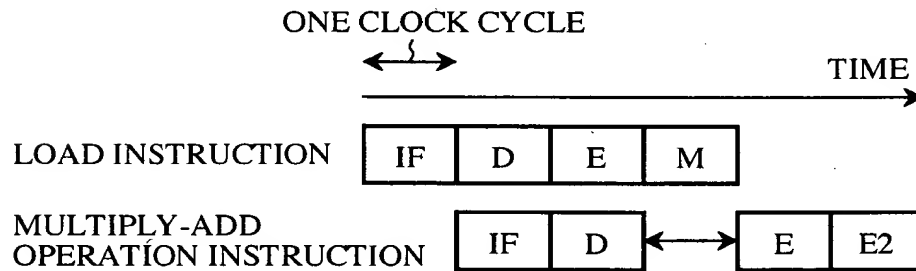


FIG. 14

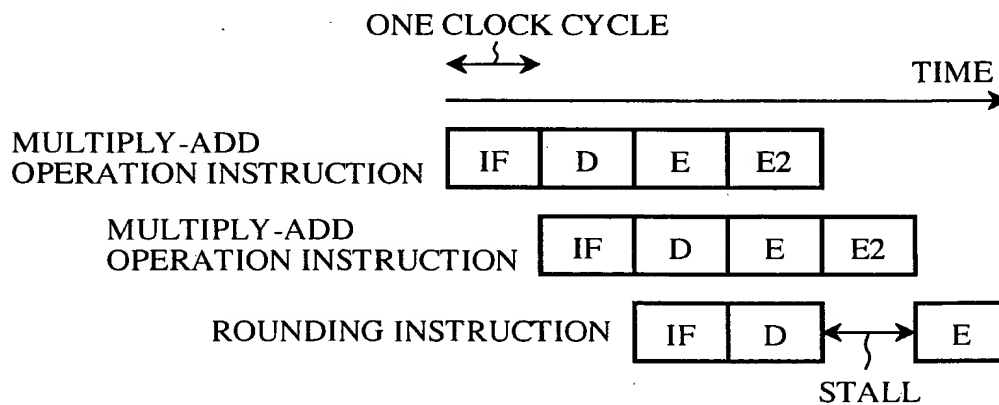




FIG.15

BIT NUMBER REP Rsrc1, Rsrc2, disp16

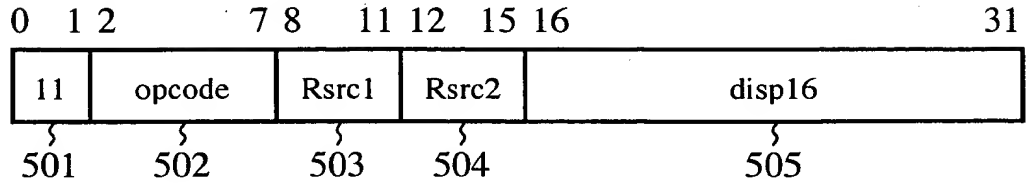


FIG.16

```

AND3    R11,R10,#h'0003                ; I1
LD2W    R0,@R8+      ||  SRLI    R10,#2    ; I2
LD2W    R4,@R9+      ||  NOP                ; I3
LD2W    R2,@R8+      ||  CLRAC   A0         ; I4

REP      R11,R10,rep_end                ; I5

LD2W    R6,@R9+      ||  MAC     A0,R0,R4   ; I6
LD2W    R0,@R8+      ||  MAC     A0,R1,R5   ; I7
LD2W    R4,@R9+      ||  MAC     A0,R2,R6   ; I8
rep_end :
LD2W    R2,@R8+      ||  MAC     A0,R3,R7   ; I9

RACHI   R0,A0,#0      ||  NOP                ; I10
:                                               ; I11
:                                               ;:

```

FIG.17

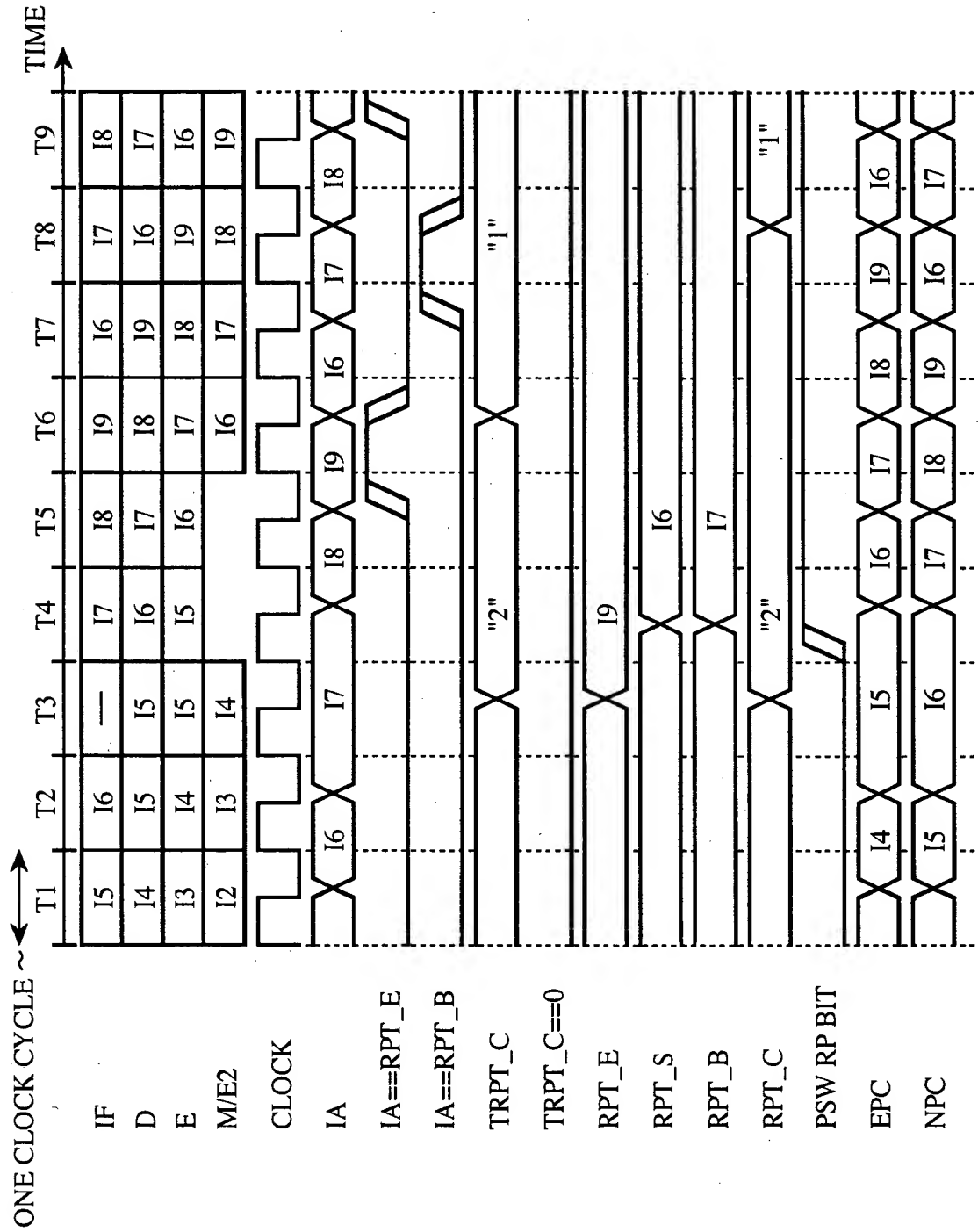


FIG. 18

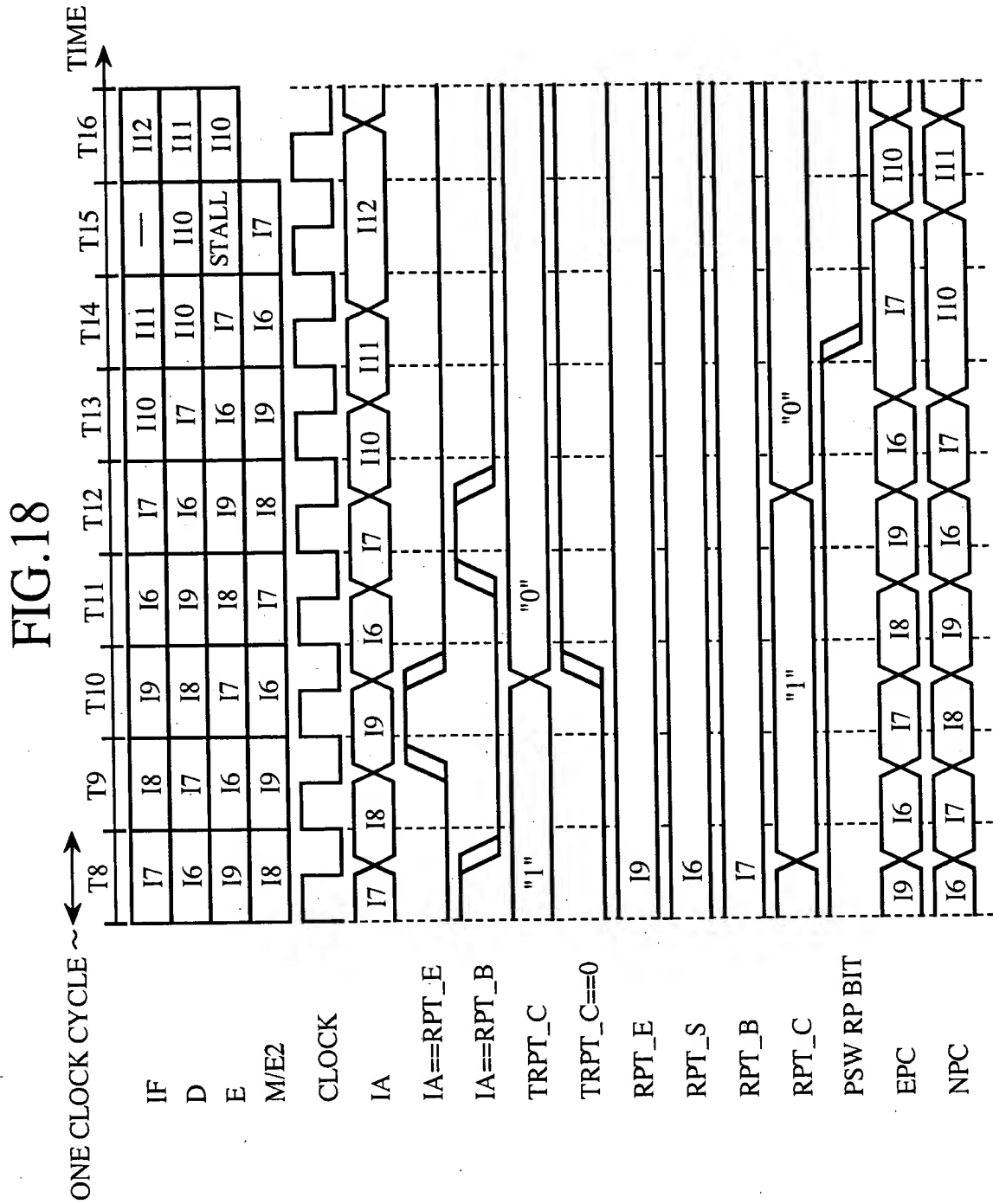


FIG.19

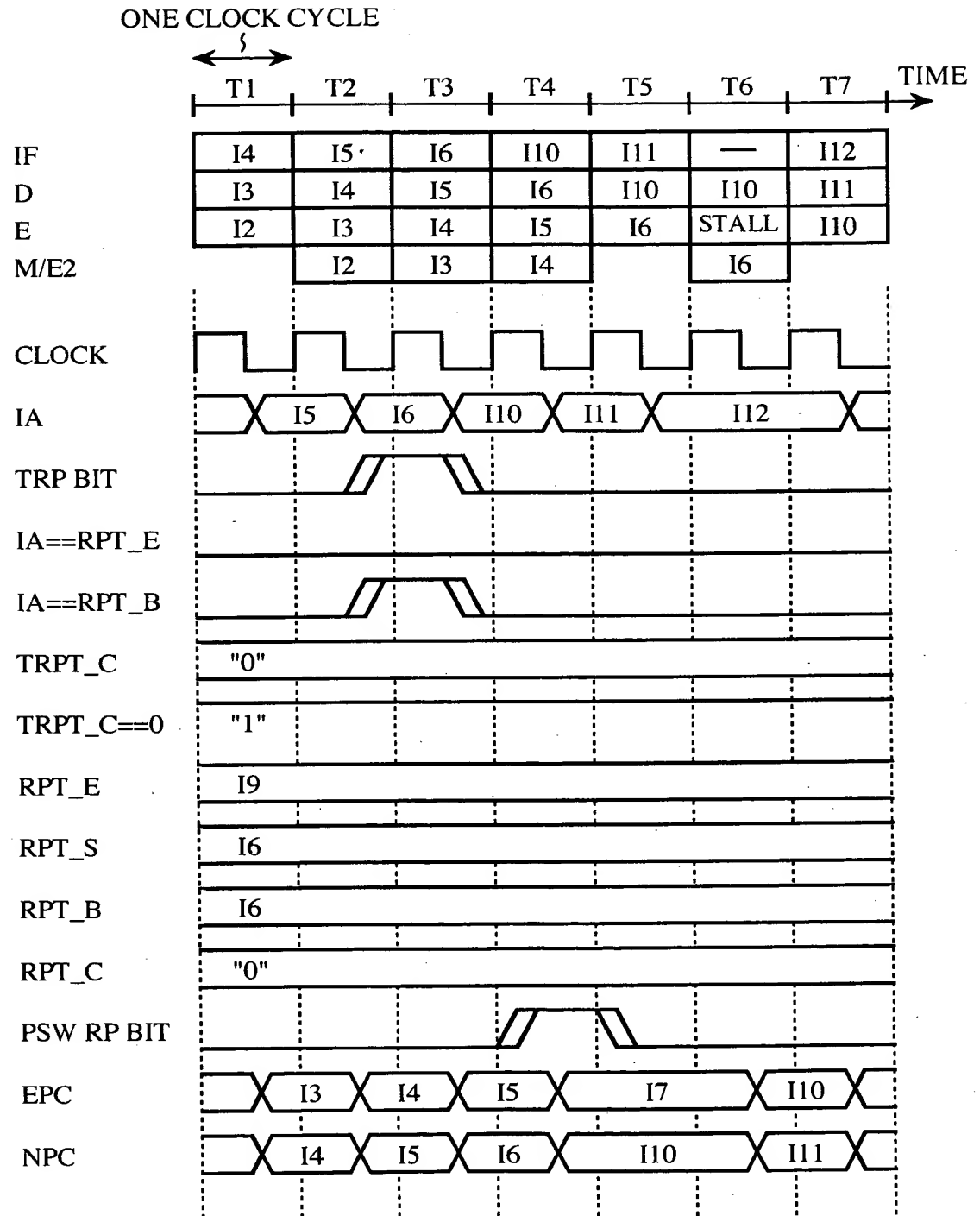


FIG.20

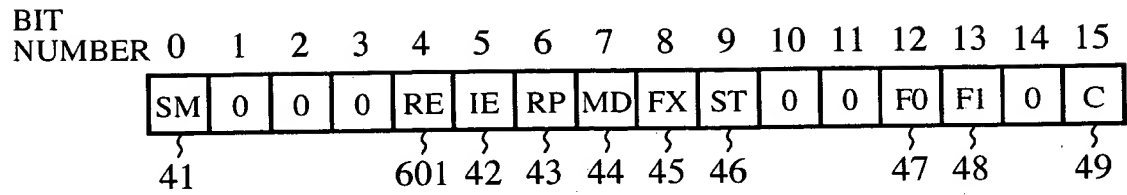


FIG.25

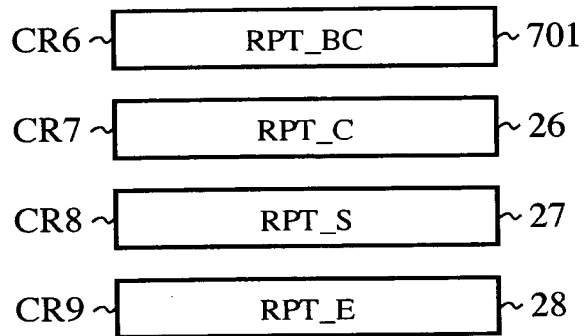


FIG.29

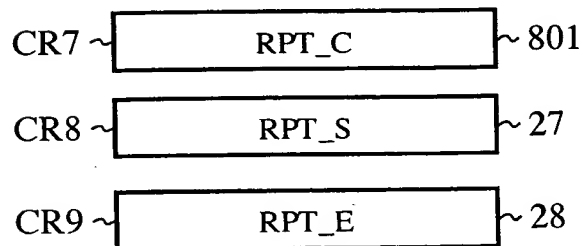


FIG.21

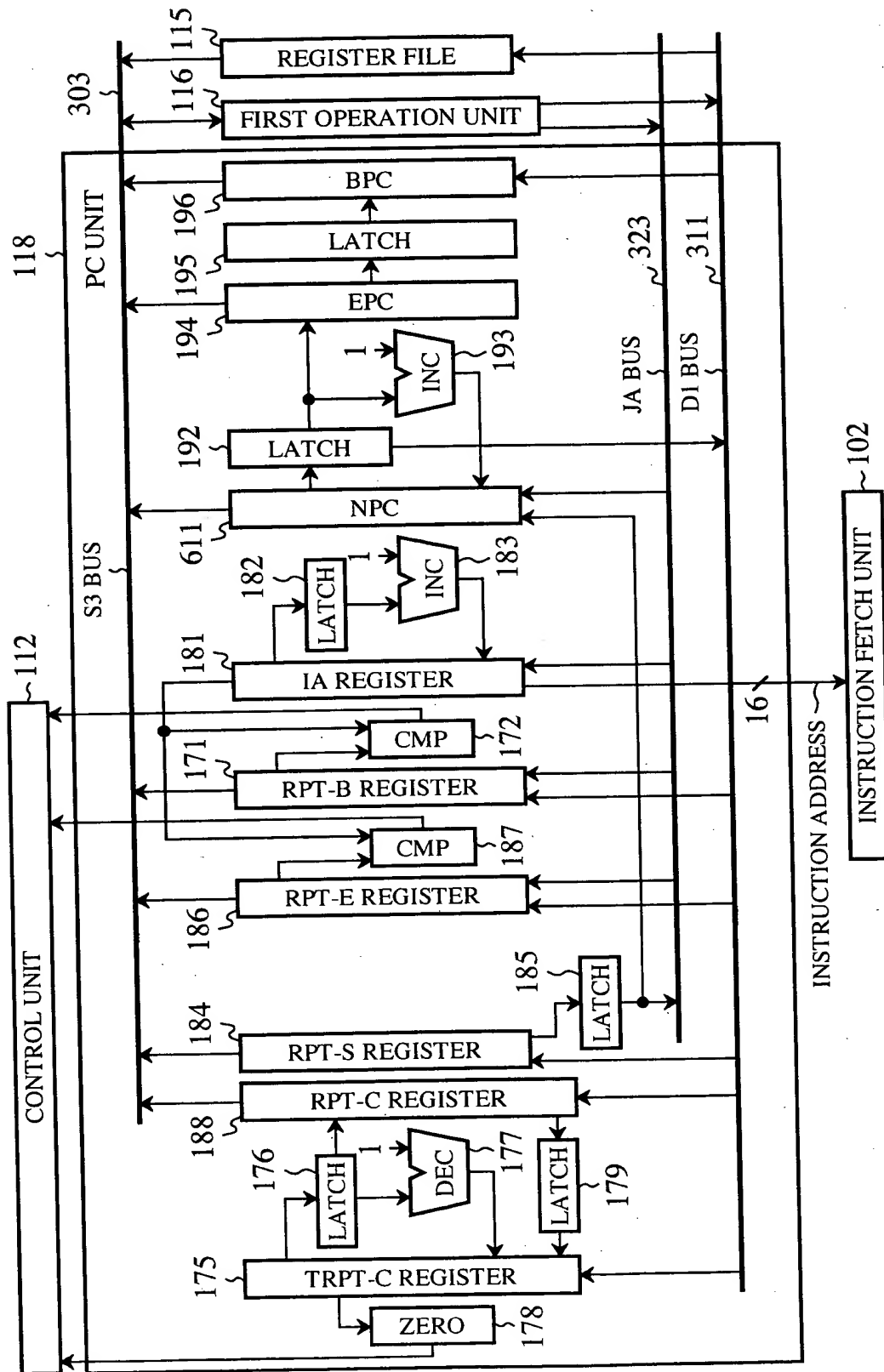


FIG. 22

FIG. 22

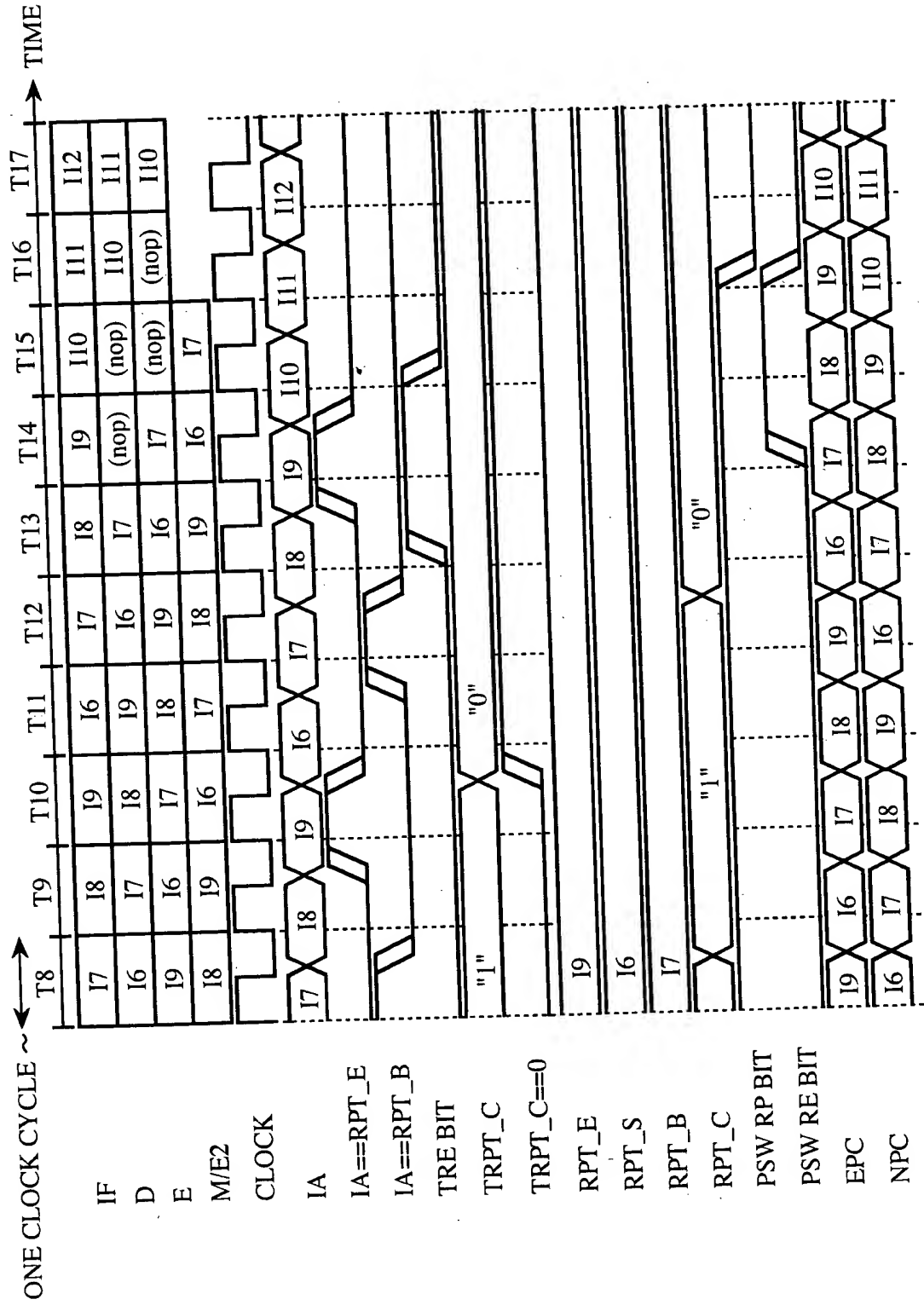


FIG.23

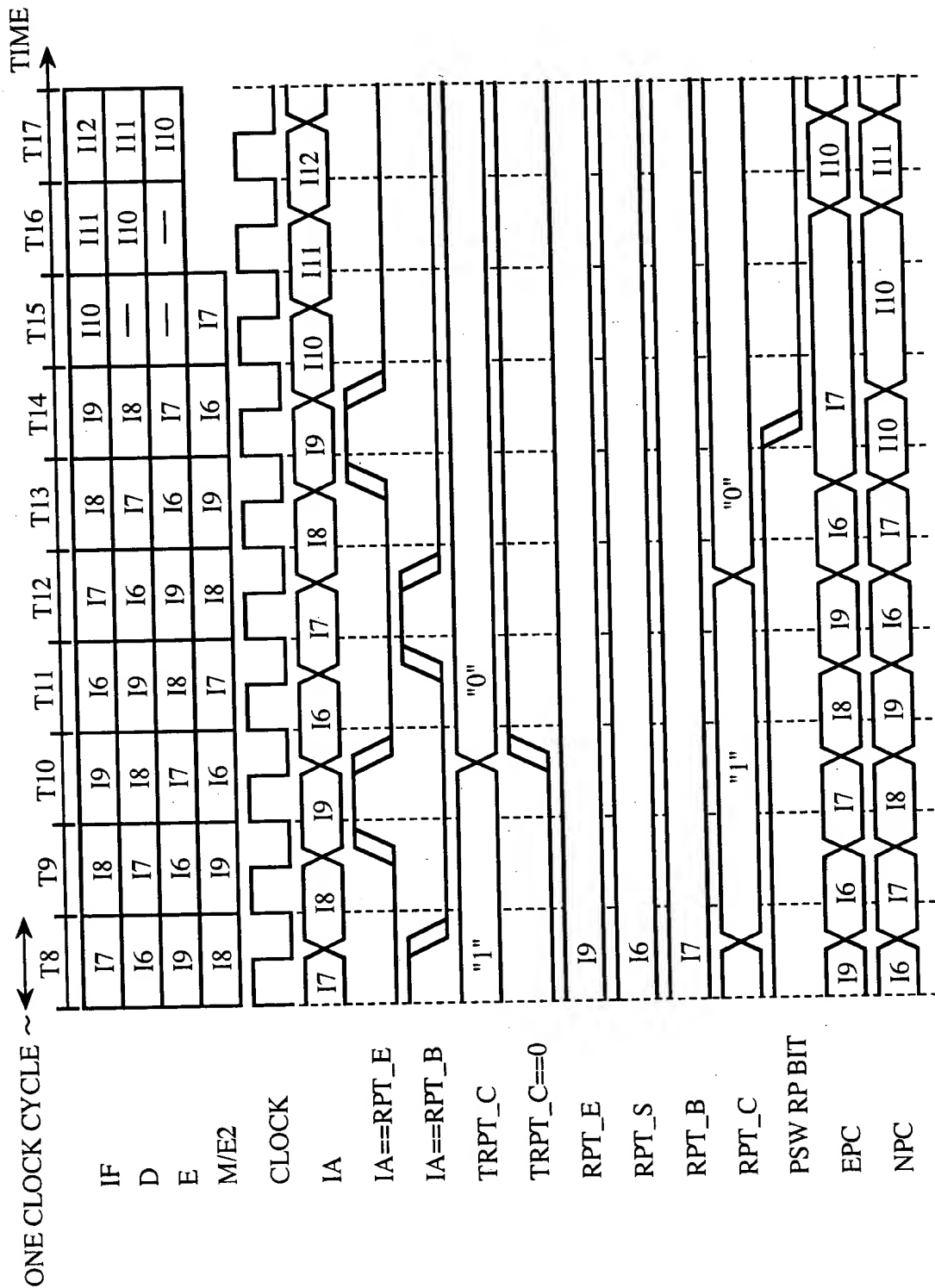




FIG.24

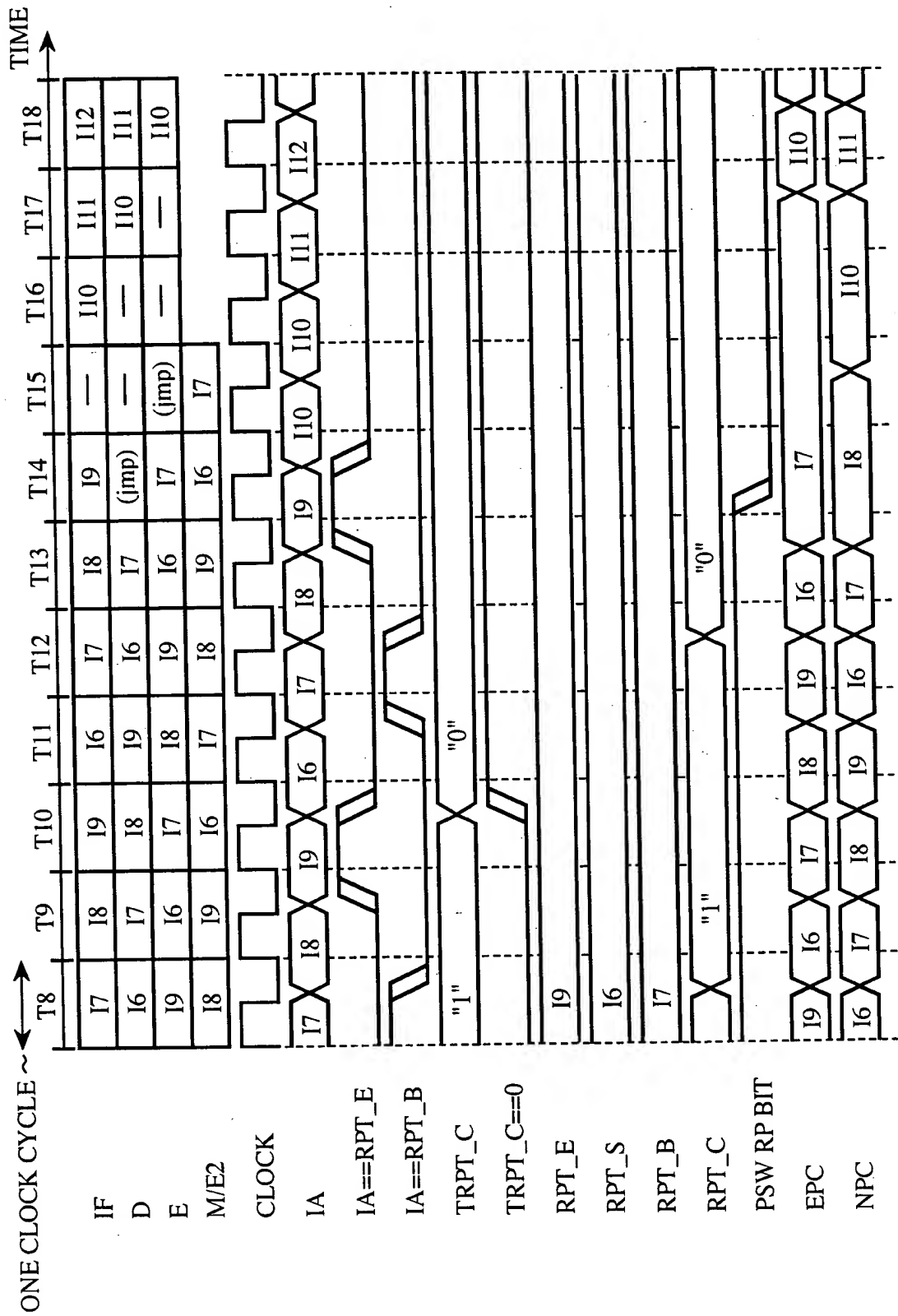


FIG. 26

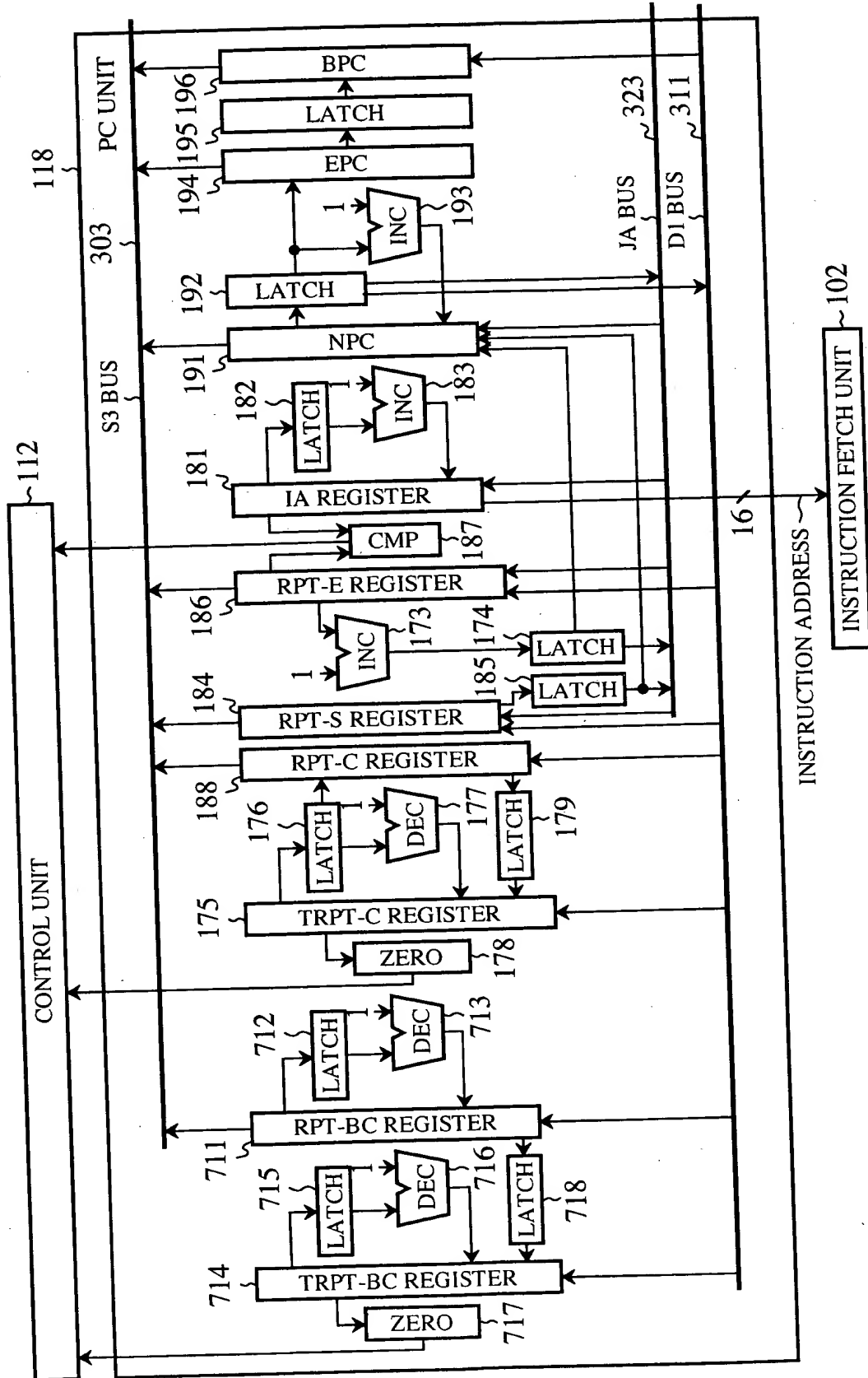


FIG. 27

FIG.27

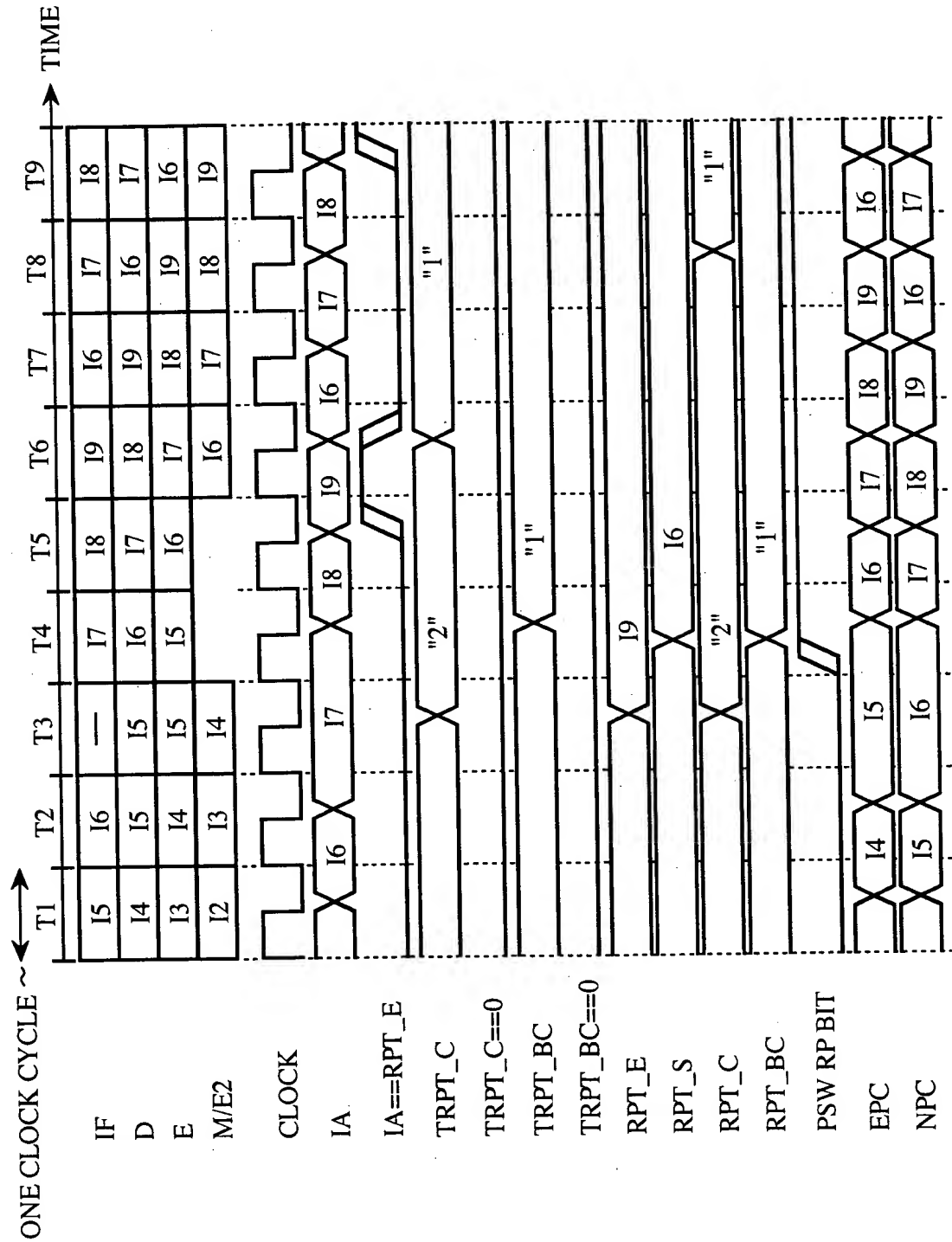
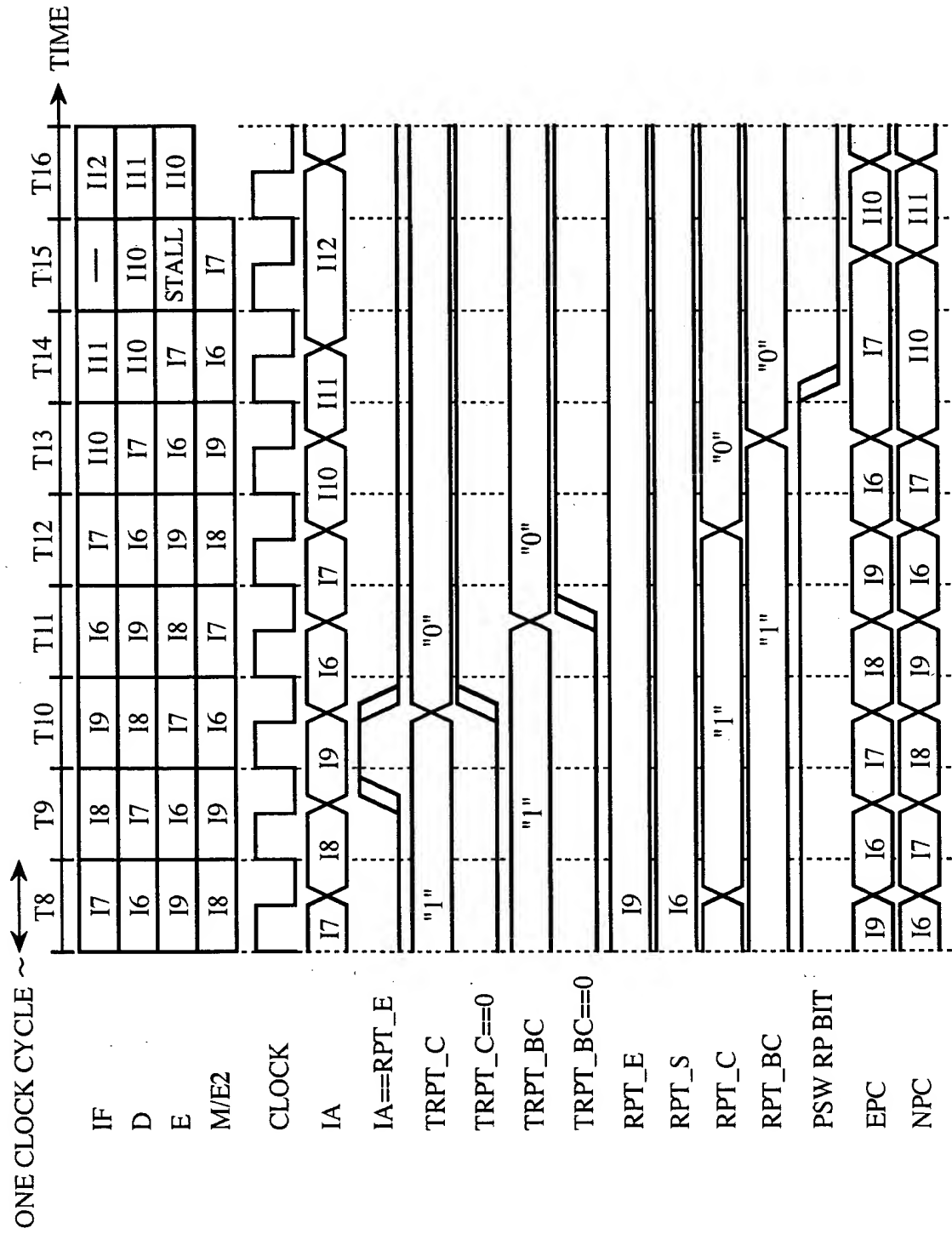


FIG.28



The diagram illustrates the internal structure of the instruction fetch unit, organized into three main functional blocks: CONTROL UNIT, PC UNIT, and INSTRUCTION FETCH UNIT.

- CONTROL UNIT (Left):** Contains control logic and registers. Key components include:
  - TRPT-C REGISTER (814):** Receives a 16-bit instruction address and provides a control signal to the RPT-C REGISTER.
  - RPT-C REGISTER (811):** Receives control signals and provides a 1-bit output to the RPT-S REGISTER.
  - RPT-S REGISTER (184):** Receives a 1-bit control signal and provides a 1-bit output to the RPT-E REGISTER.
  - RPT-E REGISTER (186):** Receives a 1-bit control signal and provides a 1-bit output to the IA REGISTER.
  - IA REGISTER (181):** Receives a 1-bit control signal and provides a 1-bit output to the NPC.
  - INC (173):** Increments the output of the RPT-S REGISTER.
  - DEC (813):** Decrements the output of the RPT-C REGISTER.
  - DEC (816):** Decrements the output of the RPT-C REGISTER.
  - ONE (817):** Provides a constant logic '1' to the TRPT-C REGISTER.
- PC UNIT (Middle):** Manages the program counter and instruction pointers. Key components include:
  - NPB (192):** Receives a 1-bit control signal and provides a 1-bit output to the NPC.
  - LATCH (195):** Latches the output of the NPB.
  - INC (193):** Increments the output of the LATCH.
  - EPC (194):** Receives a 1-bit control signal and provides a 1-bit output to the LATCH.
  - LATCH (196):** Latches the output of the EPC.
  - BPC (196):** Receives a 1-bit control signal and provides a 1-bit output to the LATCH.
- INSTRUCTION FETCH UNIT (Right):** Retrieves instructions from memory. Key components include:
  - REGISTER FILE (115):** Provides data to the FIRST OPERATION UNIT.
  - FIRST OPERATION UNIT (116):** Performs operations on data from the REGISTER FILE.
  - JA BUS (323):** Provides a 16-bit instruction address to the INSTRUCTION FETCH UNIT.
  - DI BUS (311):** Provides a 16-bit instruction address to the INSTRUCTION FETCH UNIT.

The diagram shows the flow of data and control signals between these units, with specific bit widths (e.g., 16, 1, 303) indicated for various buses and registers.

INSTRUCTION ADDRESS → INSTRUCTION FETCH UNIT ~ 102

FIG.31

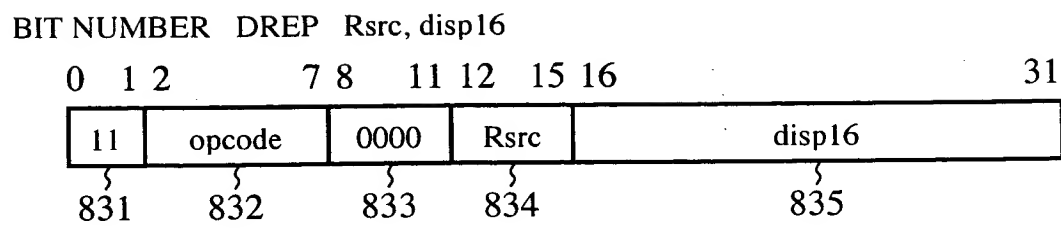


FIG.32

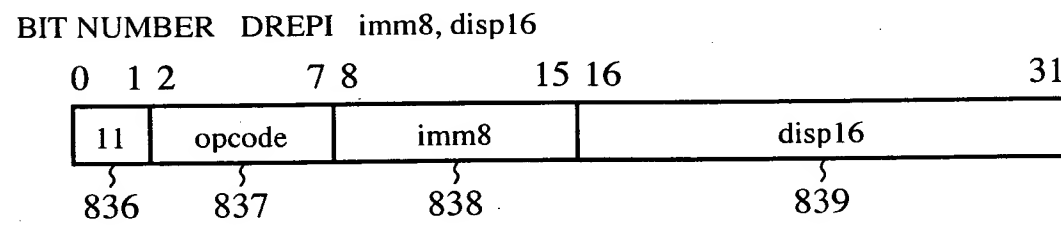


FIG.33

```
LD2W    R0,@R8+           ; I1a
LD2W    R4,@R9+           ; I1b

DREP    R10,rep_end       ; I2

LD2W    R2,@R8+    || CLRAC    A0      ; I3

rep_start :

LD2W    R6,@R9+    || MAC    A0,R0,R4    ; I4
LD2W    R0,@R8+    || MAC    A0,R1,R5    ; I5
LD2W    R4,@R9+    || MAC    A0,R2,R6    ; I6

rep_end :

LD2W    R2,@R8+    || MAC    A0,R3,R7    ; I7

RACHI   R0,A0,#0    || NOP            ; I8
:                                               ; I9
:                                               ;:
```

TOP SECRET

FIG.34

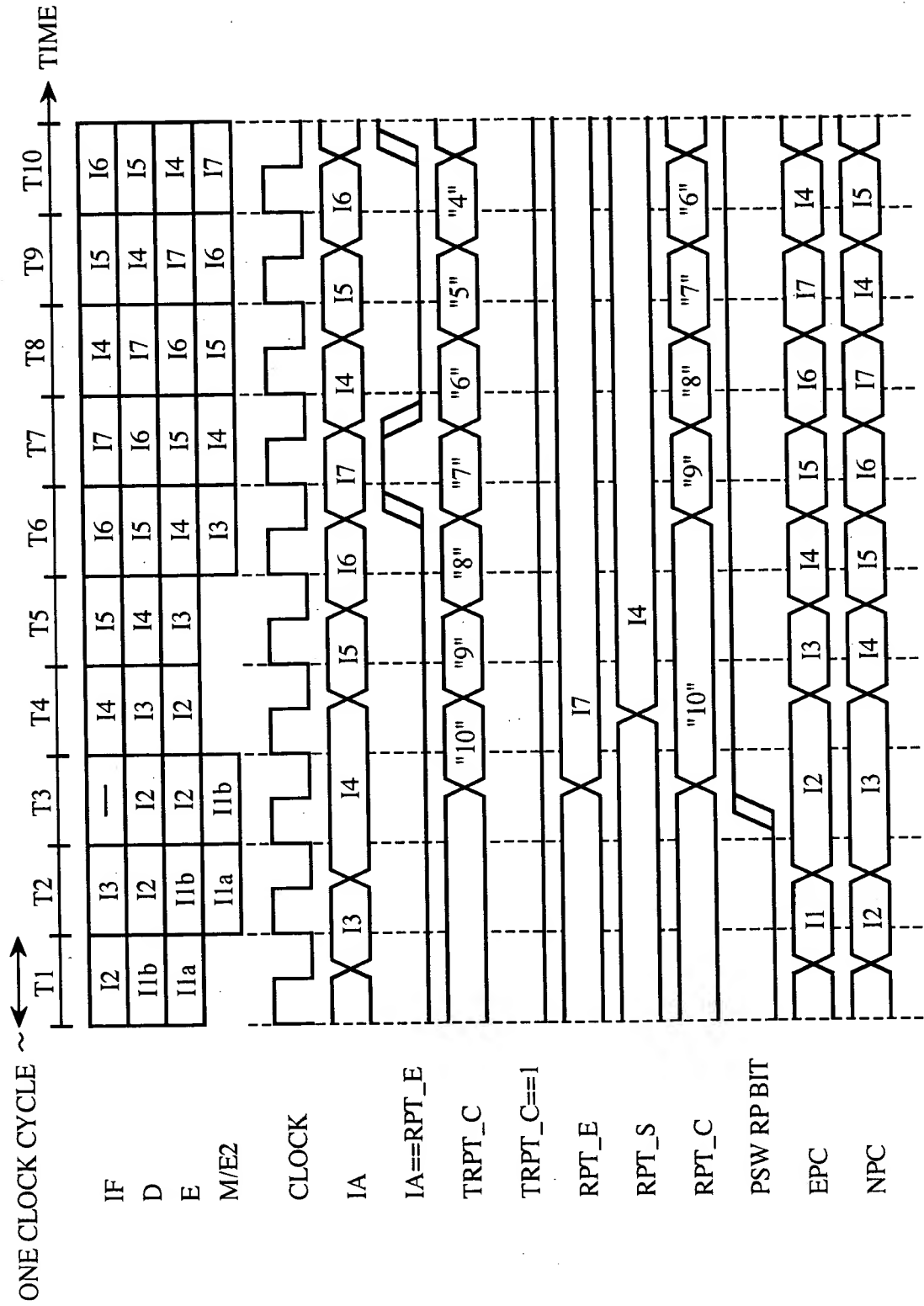


FIG. 35

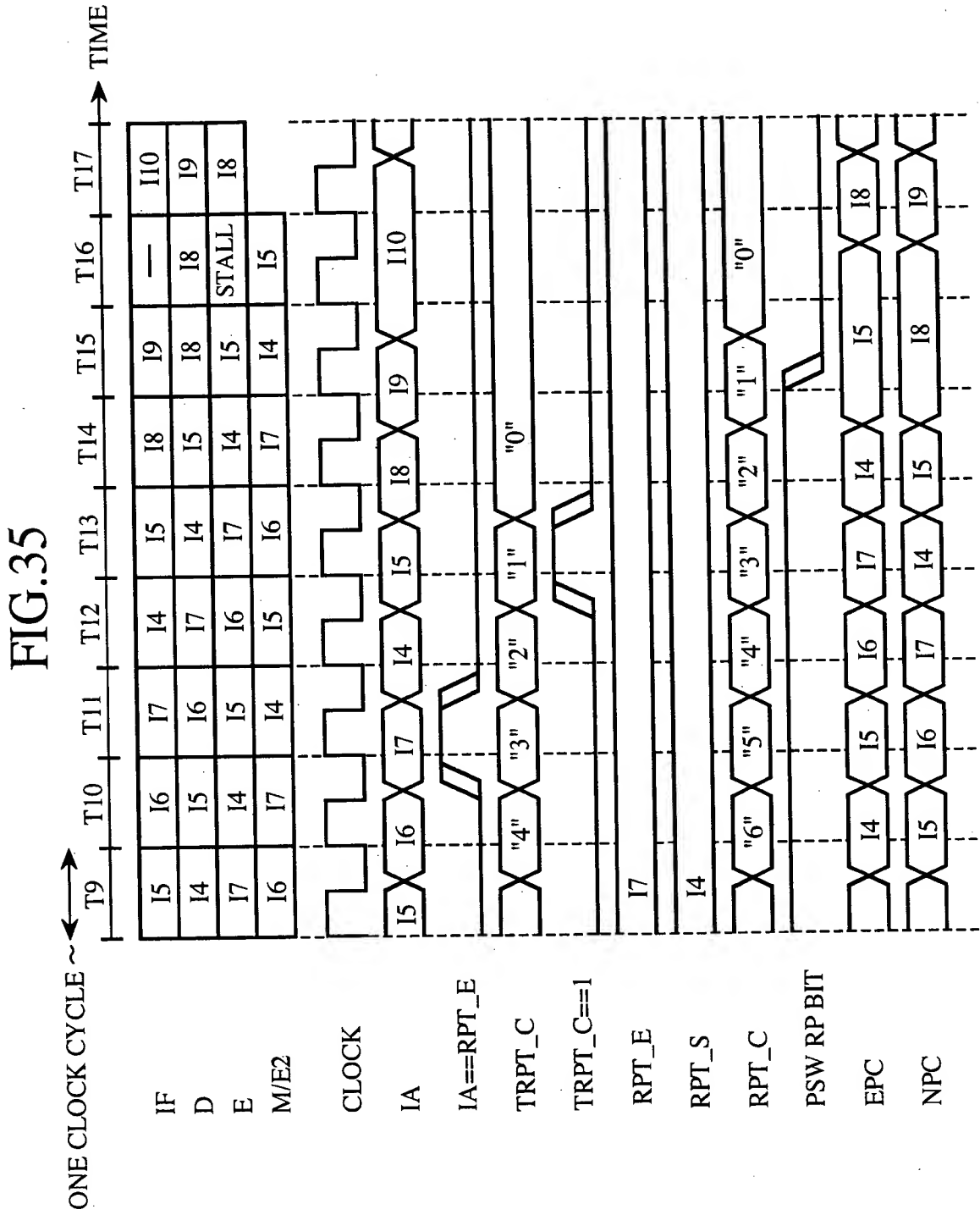
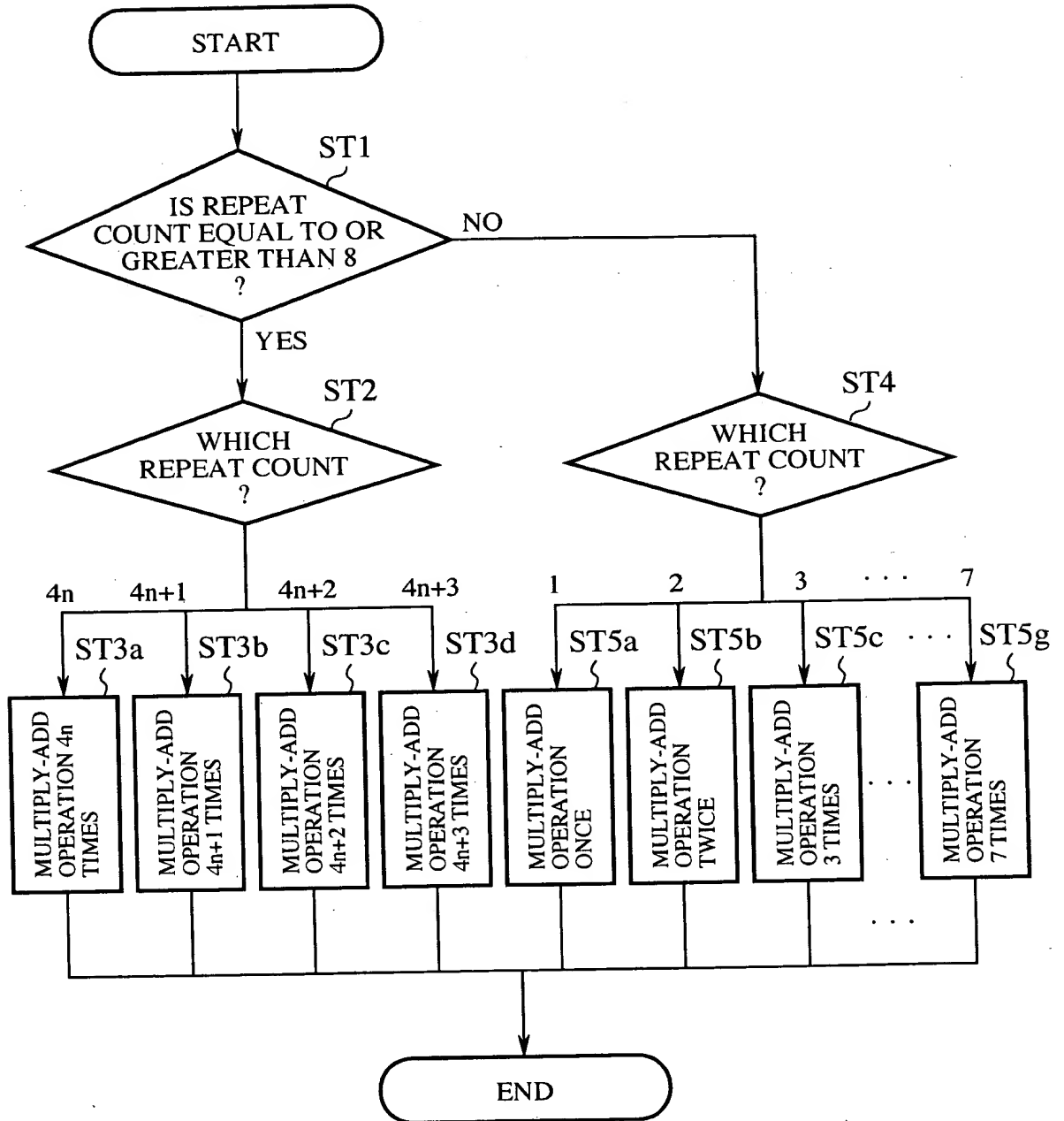




FIG.36 (PRIOR ART)



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